# JUMPERS AND STUFF

| REF | TYPE | DESCRIPTION | PAGE |
|---|---|---|---|
| JP1 | BLOB | KEYBOARD RESET | 7 |
| JP2 | BLOB | CD VS. DB ADDRESS MAP | 2 |
| JP3 | BLOB | EXPANSION RAS SELECT | 3 |
| JP4 | BLOB | BYPASS 2M-BYTE DECODER | 3 |
| | | | |
| JP7 | BLOB | EXPANSION/TICK OPTION | 6,8 |
| JP8 | BLOB | LIGHT PEN PORT SELECT | 5 |
| JP9 | BLOB | ON-BOARD RTC BYPASS | 8 |
| JP10 | BLOB | RS232 AUDIO I/O CUTOUT | 5 |
| JP11 | BLOB | TTL VS RS170 COMP SYNC | 4 |

# CONNECTORS

| REF | TYPE | DESCRIPTION | PAGE |
|---|---|---|---|
| CN1 | DB9P | MOUSE/JOYSTICK 1 | 5 |
| CN2 | DB9P | MOUSE/JOYSTICK 2 | 5 |
| CN3 | RCA-J | RIGHT AUDIO OUTPUT | 5 |
| CN4 | RCA-J | LEFT AUDIO OUTPUT | 5 |
| CN5 | DB23S | EXTERNAL FLOPPY | 7 |
| CN6 | DB25P | RS232 SERIAL PORT | 5 |
| CN7 | DB25S | PARALLEL PRINTER PORT | 6 |
| CN8 | SQ DIN | POWER SUPPLY CONNECTOR | 10 |
| CN9 | DB23P | VIDEO OUTPUT | 4 |
| CN10 | RCA-J | COMPOSITE VIDEO | 4 |
| CN11 | DIL-34 | INTERNAL FLOPPY SIGNAL | 7 |
| CN12 | SIL-4 | INTERNAL FLOPPY POWER | 7 |
| CN13 | SIL-8 | KEYBOARD CONNECTOR | 7 |
| | | | |
| P1 | EDGE86 | EXPANSION CONNECTOR | 9 |
| | | | |
| P9 | RA-56H | MEM. EXP. MAIN-BOARD | 8 |

# REVISION HISTORY

| REV | DESCRIPTION | DATE | APPVL | MANAGER |
|---|---|---|---|---|
| - | FOR OLDER REVISION 3/5 BOARDS | | | |
| | SEE SCHEMATIC 312511-01 | | | |
| - | FOR OLDER REVISION 6A/7 BOARDS | | | |
| | SEE SCHEMATIC 312007-01 | | | |
| | | | | |
| 0 | PCB REVISION 8 PROTOTYPE | 04/13/91 | ORR | |

# ECC LOG

| ECO NUMBER | DESCRIPTION | DATE |
|---|---|---|
| | | |
| | | |
| | | |
| | | |

# SIGNAL GLOSSARY

| SIGNAL | DESCRIPTION (AREA) | PAGES |
|---|---|---|
| 28MHZ | 28.63636 MHZ MASTER CLOCK | 2 |
| 7MHZ | 7.15909 MHZ PROCESSOR CLOCK | 2,4,9,10 |
| A[23:1] | PROCESSOR ADDRESS BUS (68000) | 2,6,8,9 |
| ACK | DATA ACKNOWLEDGE (PARALLEL PORT) | 6 |
| AS | ADDRESS STROBE (68000) | 2,9 |
| AUDIN | AUDIO INPUT (RS232 PORT) | 5,6 |
| AUDOUT | AUDIO OUTPUT (RS232 JACK) | 5,6 |
| BEER | BUS ERROR (68000) | 2,9 |
| BG | BUS GRANT (68000) | 2,9 |
| BGACK | BUS GRANT ACKNOWLEDGE (68000) | 2,9 |
| BLISS | BLITTER SLOWDOWN (CHIPS) | 2 |
| BLIT | CHIP MEMORY ACCESS (CHIPS) | 2 |
| BR | BUS REQUEST (68000) | 2,9 |
| BUSY | DEVICE BUSY (PARALLEL PORT) | 6 |
| CASL/U | COLUMN ADDRESS STROBE (DRAM) | 2,3 |
| CCK/CCKQ | COLOR CLOCK / QUADRATURE (CHIPS) | 2-5,9,10 |
| CDAC | 7.15909 MHZ QUADRATURE CLOCK (CHIPS) | 2,4,9,10 |
| CHNG | MEDIA CHANGE (FLOPPY) | 6,7 |
| CLKRD/WR | READ-TIME CLOCK READ / WRITE (RTC) | 2,8 |
| COMP | MONOCHROME COMPOSITE VIDEO (VIDEO) | 4 |
| CSYNC | COMPOSITE SYNC (VIDEO) | 2,4 |
| CTS | CLEAR TO SEND (RS232 PORT) | 6 |
| D[15:0] | PROCESSOR DATA BUS (68000) | 2,6,8,9 |
| DIR | STEP DIRECTION (FLOPPY) | 6,7 |
| DKRD | DISK READ DATA (FLOPPY) | 5,7 |
| DKWD | DISK WRITE DATA (FLOPPY) | 5,7 |
| DKWE | DISK WRITE ENABLE (FLOPPY) | 5,7 |
| DMAL | CHIP DMA REQUEST LINE (CHIPS) | 2,5 |
| DRA[8:0] | DRAM ADDRESS BUS (DRAM) | 2,3 |
| DRD[15:0] | DRAM DATA BUS (DRAM) | 2-5,8,9 |
| DSR | DATA SET READY (RS232 PORT) | 6 |
| DTACK | DATA TRANSFER ACKNOWLEDGE (68000) | 2,9 |
| DTR | DATA TERMINAL READY (RS232 PORT) | 6 |
| E | PERIPHERAL ENABLE CLOCK (68000) | 2,6,9 |
| EXTICK | EXPANSION PRESENT / RTC TICK | 2,6,8,9 |
| FC[2:0] | FUNCTION CODE (68000) | 2,9 |
| FIREO/1 | FIRE BUTTON 0/1 (JOYSTICKS) | 5,6 |
| HLT | PROCESSOR HALT (68000) | 2,9 |
| HSYNC | HORIZONTAL SYNC (VIDEO) | 2,4,6 |
| INDEX | INDEX PULSE (FLOPPY) | 6,7 |
| INT[2,3,6] | INTERRUPT REQUEST (CHIPS) | 2,5,6,9 |
| IORESET | I/O RESET | 6,7,9 |
| IPL[2:0] | INTERRUPT PRIORITY LEVEL (68000) | 2,5,9 |
| KBCLOCK | KEYBOARD CLOCK (KEYBOARD) | 6,7 |
| KBDATA | KEYBOARD DATA (KEYBOARD) | 6,7 |
| KBRESET | KEYBOARD RESET (KEYBOARD) | 7 |
| LDS/UDS | UPPER / LOWER DATA STROBES (68000) | 2,9 |
| LED | POWER ON LED / AUDIO FILTER DISABLE | 5,6,7 |
| LEFT/RIGHT | LEFT RIGHT AUDIO (AUDIO) | 5 |

| SIGNAL | DESCRIPTION (AREA) | PAGES |
|---|---|---|
| LPEN | LIGHT PEN TRIGGER (JOYSTICKS) | 2,5 |
| MTR | MOTOR ON (FLOPPY) | 6,7 |
| MTR0 | MOTOR ON - DRIVE 0 (FLOPPY) | 7 |
| MOV/MOH | MOUSE 0 QUADRATURE V/H (JOYSTICKS) | 4,5 |
| M1V/M1H | MOUSE 1 QUADRATURE V/H (JOYSTICKS) | 4,5 |
| OVL | OVERLAY ROM OVER RAM | 2,6,9 |
| OVR | OVERRIDE SYSTEM DECODING | 2,9 |
| PIXELSW | GENLOCK PIXEL SWITCH (VIDEO) | 4 |
| POT0X/0Y | POT LINES 0 X/Y (JOYSTICKS) | 5 |
| POT1X/1Y | POT LINES 1 X/Y (JOYSTICKS) | 5 |
| POUT | PAPER OUT (PARALLEL PORT) | 6 |
| PPD[7:0] | PARALLEL PORT DATA (PARALLEL PORT) | 6 |
| RAMEN | RAM ENABLE (CHIPS) | 2 |
| REGEN | CHIP REGISTER ENABLE (CHIPS) | 2 |
| RAS0/1 | ROW ADDRESS STROBE (DRAM) | 2,3 |
| RDY | DRIVE READY (FLOPPY) | 6,7 |
| RESET | GENERAL RESET | 6,9 |
| RGA[8:1] | REGISTER ADDRESS BUS (CHIPS) | 2,4,5 |
| R/G/B | RED / GREEN / BLUE (VIDEO) | 4 |
| RI | RING INDICATE (RS232 PORT) | 6 |
| ROMEN | ROM ENABLE (ROM) | 2,8 |
| RTS | REQUEST TO SEND (RS232 PORT) | 6 |
| RST | PROCESSOR RESET (68000) | 2,5,9 |
| RXD | RECEIVE DATA (RS232 PORT) | 5,6 |
| RW | PROCESSOR READ/WRITE (68000) | 2,6,9 |
| SEL | SELECT (PARALLEL PORT) | 6 |
| SEL[3:0] | DRIVE SELECT (FLOPPY) | 6,7 |
| SIDE | SIDE SELECT (FLOPPY) | 6,7 |
| STEP | STEP IN/OUT COMMAND (FLOPPY) | 6,7 |
| TRK0 | TRACK ZERO SENSE (FLOPPY) | 6,7 |
| TXD | TRANSMIT DATA (RS232 PORT) | 5,6 |
| VMA | VALID MEMORY ADDRESS (68000) | 2,9 |
| VPA | VALID PERIPHERAL ADDRESS (68000) | 2,9 |
| VSYNC | VERTICAL SYNC (VIDEO) | 2,4,6 |
| WE | WRITE ENABLE (DRAM) | 2,3 |
| WPROT | WRITE PROTECT SENSE (FLOPPY) | 6,7 |
| XCLK | EXTERNAL GENLOCK CLOCK (VIDEO) | 2,4 |
| XCLKEN | EXTERNAL CLOCK ENABLE (VIDEO) | 2,4,9 |
| XRDY | EXTERNAL DATA READY | 2,9 |

# KEY COMPONENTS

| REF | CHIP | DESCRIPTION | PAGE |
|---|---|---|---|
| U1 | 68000 | 68000 PROCESSOR, 8MHZ | 2 |
| U2 | 8375 | AGNUS HR | 2 |
| | | | |
| U3 | 8364 | PAULA | 5 |
| U4 | 8373 | DENISE HR | 4 |
| | 8362 | DENISE | OBS |
| U5 | 5719 | GARY | 2,7 |
| U6 | ASST | ROM 256KX16, 200 NS | 8 |
| U7-8 | 8520 | AMIGA VIA, 1 MHZ | 6 |
| U9 | 6242 | REAL TIME CLOCK | 8 |
| U14 | LF347 | BIMOS OP-AMP | 5 |
| | TL084 | BIMOS OP-AMP | ALT |
| U38 | 1488 | EIA LINE DRIVER | 6 |
| U39 | 1489 | EIA LINE RECEIVER | 6 |
| U42 | NE555 | TIMER | 7 |
| U16-19 | ASST | DRAM 256KX4, 120 NS | 3 |
| U20-23 | ASST | DRAM 256KX4, 120 NS | 3 |
| X1 | OSC | TTL 28.63636 MHZ NTSC | 2 |
| | OSC | TTL 28.37512 MHZ PAL | ALT |
| | | | |
| HY1 | ASST | VIDEO HYBRID | 4 |

A PAGE FOR SHARON AND YONNIE TO USE

COMMODORE

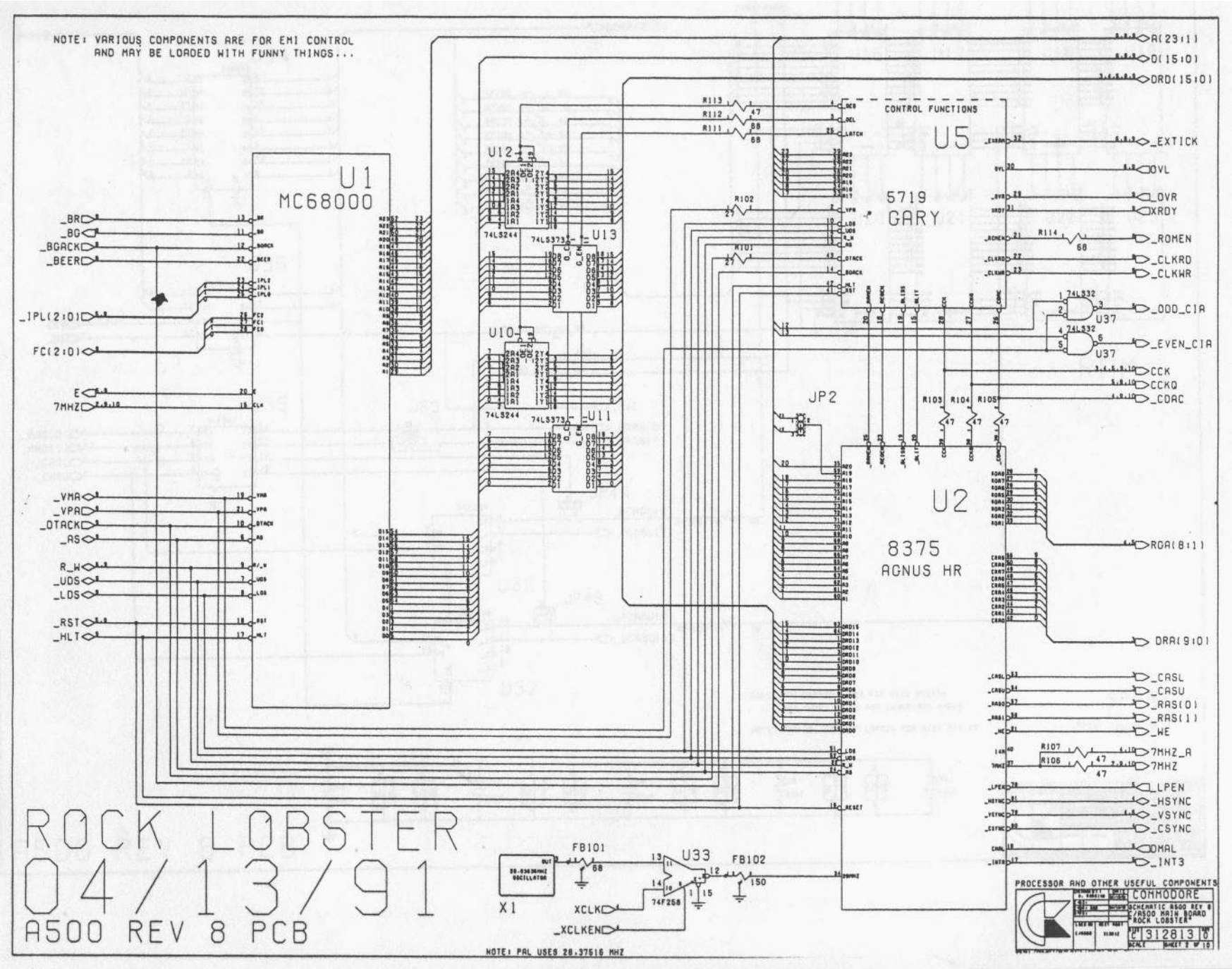
SCHEMATIC A500 REV 8
C/A500 MAIN BOARD
"ROCK LOBSTER"

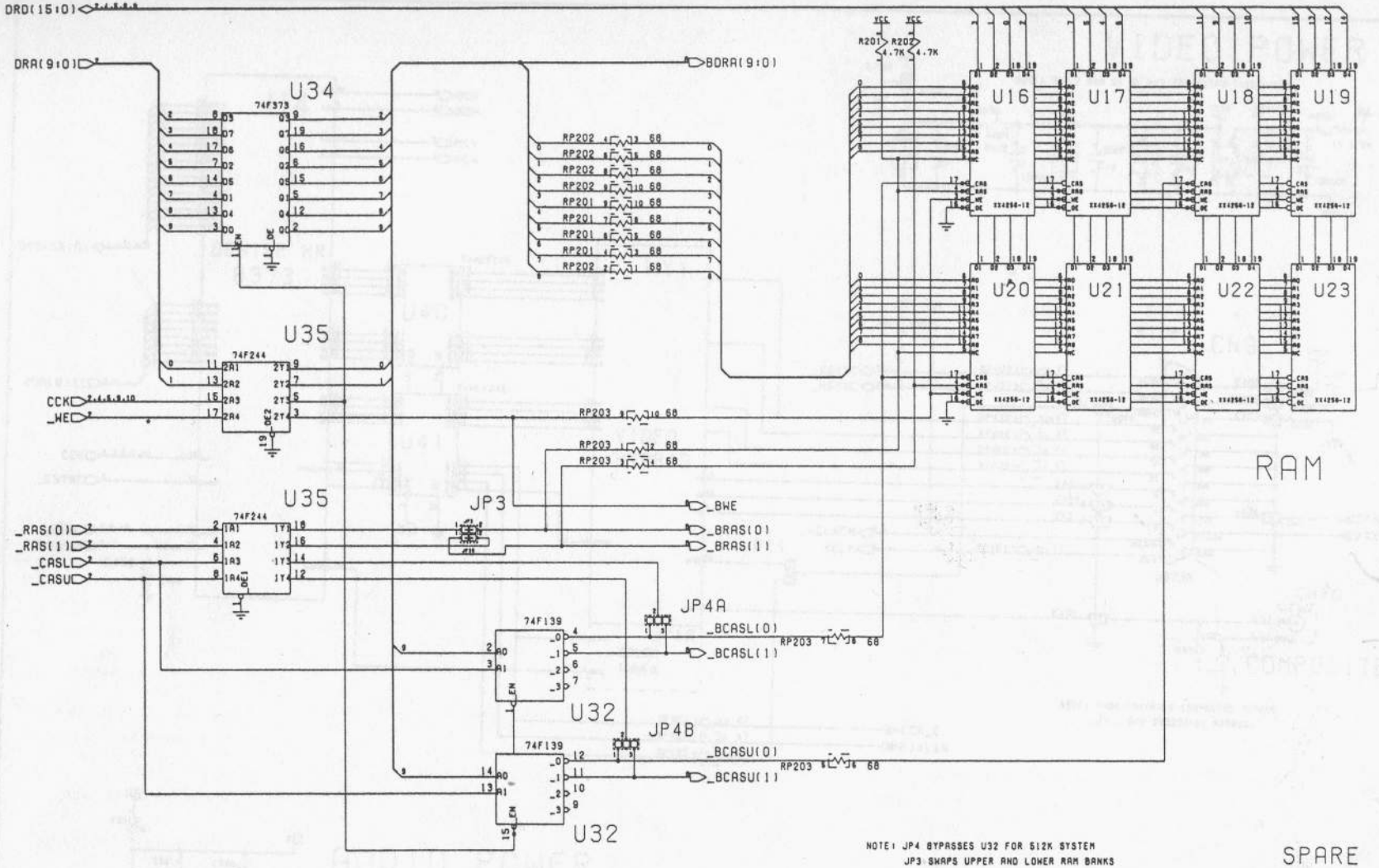
SIZE C 312813 0

SCALE

SHEET 1 OF 10

# A500 REV 8 PCB


NOTE: VARIOUS COMPONENTS ARE FOR EMI CONTROL AND MAY BE LOADED WITH FUNNY THINGS...
U1
MC68000
U2
8375
AGNUS HR
U5
5719
GARY
CONTROL FUNCTIONS
U12
U13
U10
U11
74LS244
74LS373
JP2
U37
74LS32
U33
74F258
FB101
FB102
X1
XCLK
_XCLKEN
R(23:1)
D(15:0)
DRD(15:0)
_EXTICK
OVL
_OVR
XRDY
_ROMEN
_CLKRD
_CLKWR
_ODD_CIA
_EVEN_CIA
CCK
CCKQ
_CDAC
RGA(8:1)
DRA(9:0)
_CASL
_CASU
_RAS(0)
_RAS(1)
_WE
7MHZ_A
7MHZ
_LPEN
_HSYNC
_VSYNC
_CSYNC
_MAL
_INT3
_BR
_BG
_BGACK
_BEER
_IPL(2:0)
FC(2:0)
E
7MHZ
_VMA
_VPA
_DTACK
_AS
R_W
_UDS
_LDS
_RST
_HLT
PROCESSOR AND OTHER USEFUL COMPONENTS
COMMODORE
SCHEMATIC A500 REV 8
C/A500 MAIN BOARD
"ROCK LOBSTER"
C 312813 0
ROCK LOBSTER
04/13/91
A500 REV 8 PCB
NOTE: PAL USES 28.37516 MHZ




A500 REV 8 PCB

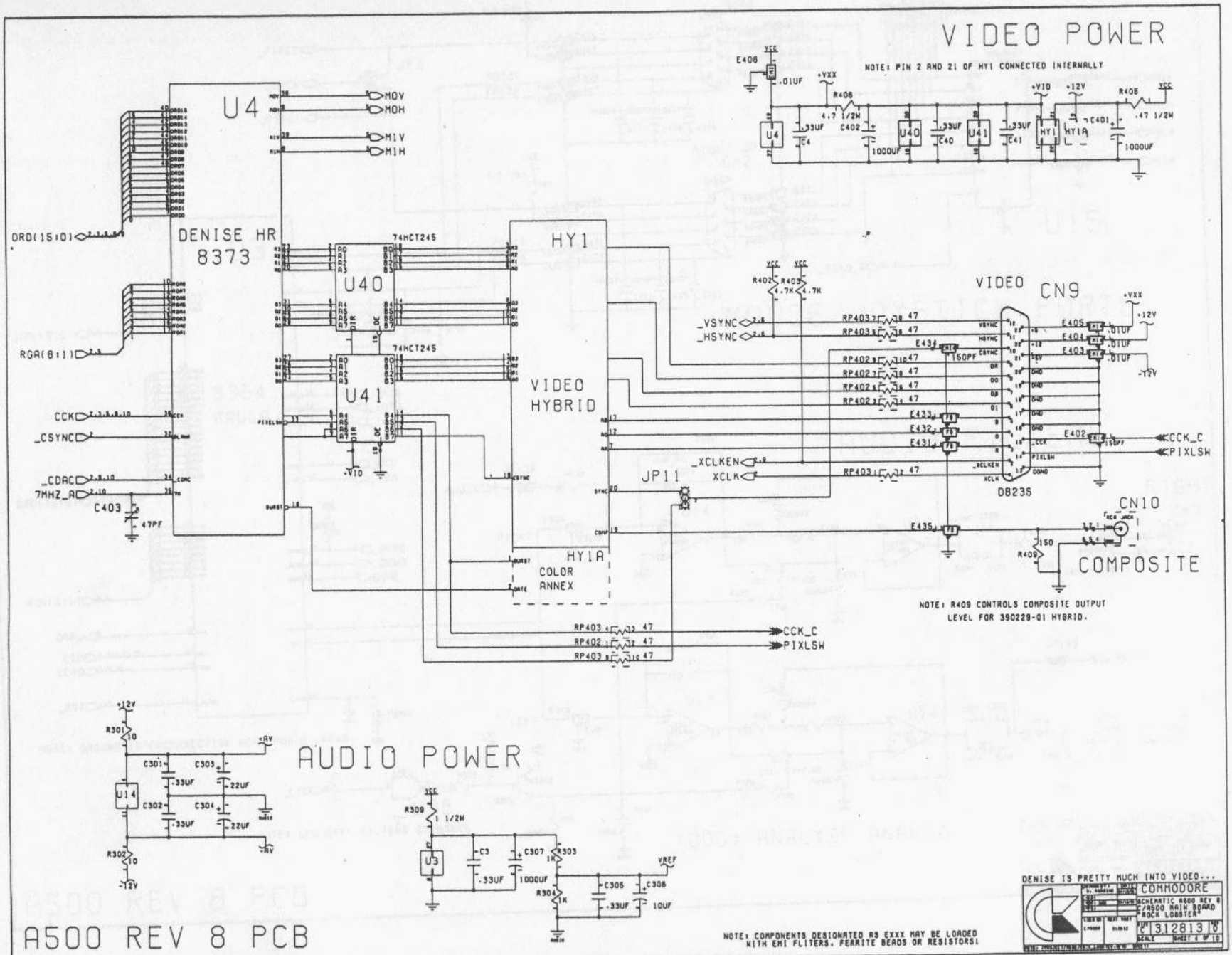
MEMORY AND...WELL, I USED TO REMEMBER

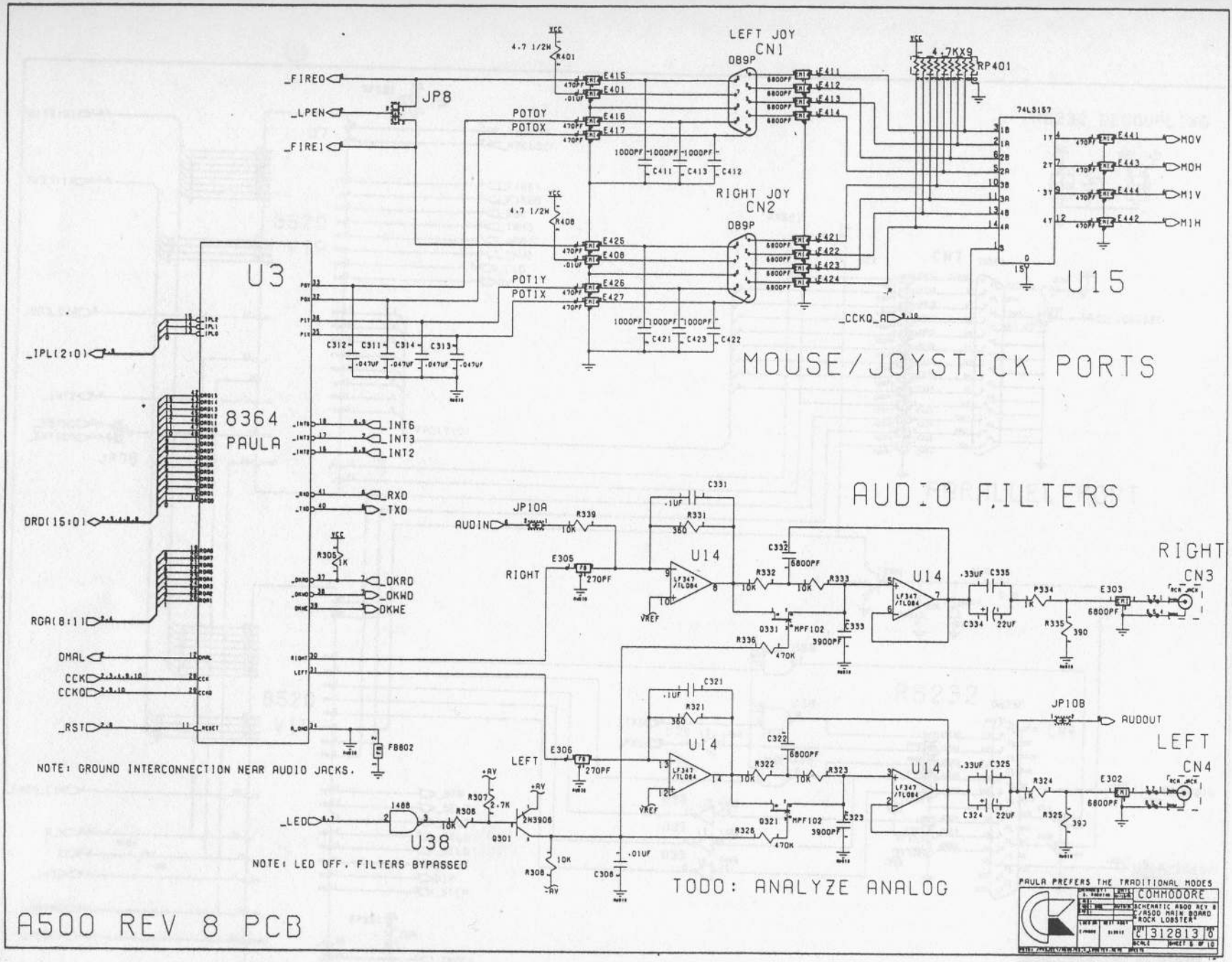
COMMODORE

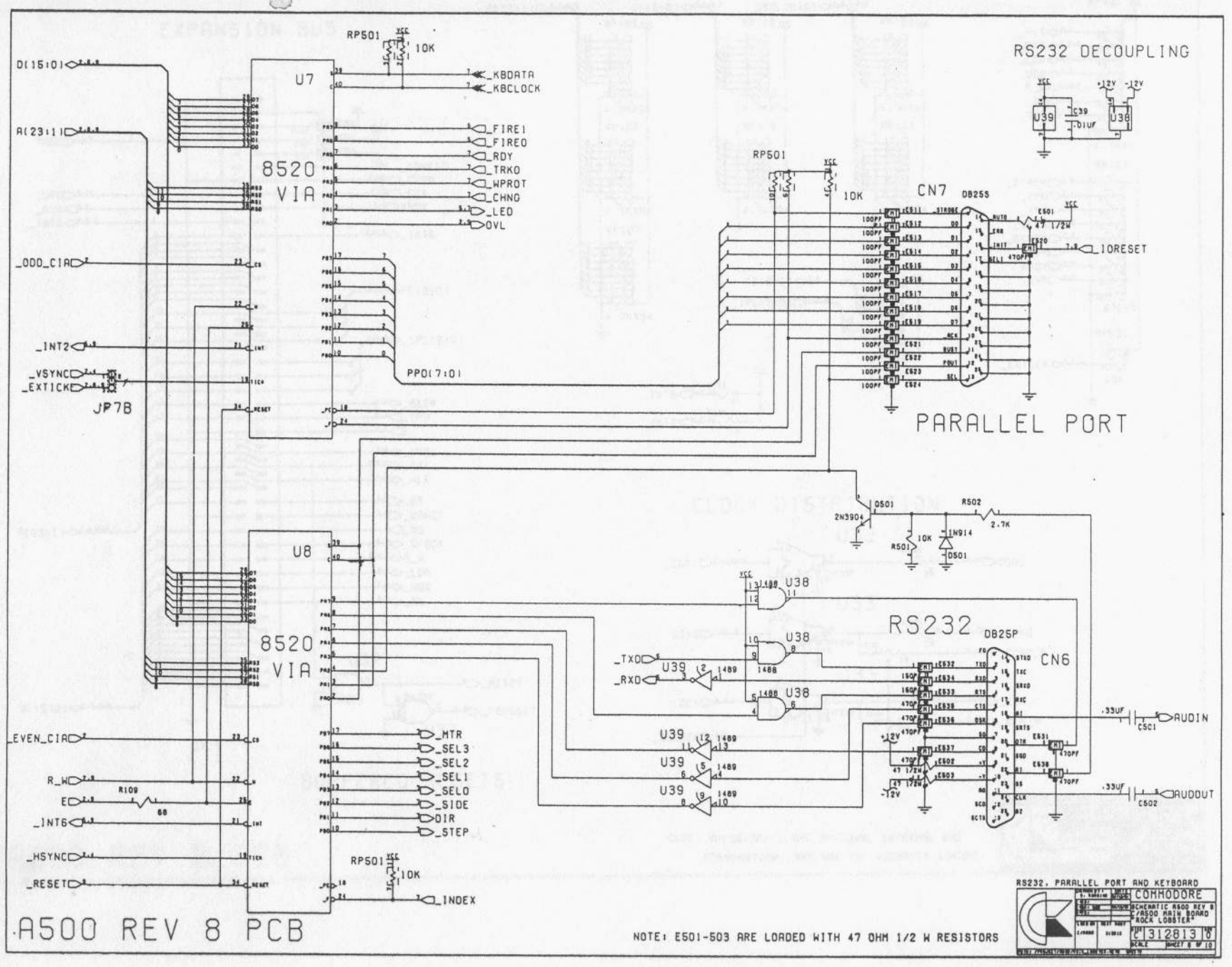
SCHEMATIC A500 REV 8
C/A500 MAIN BOARD
"ROCK LOBSTER"

312813 0

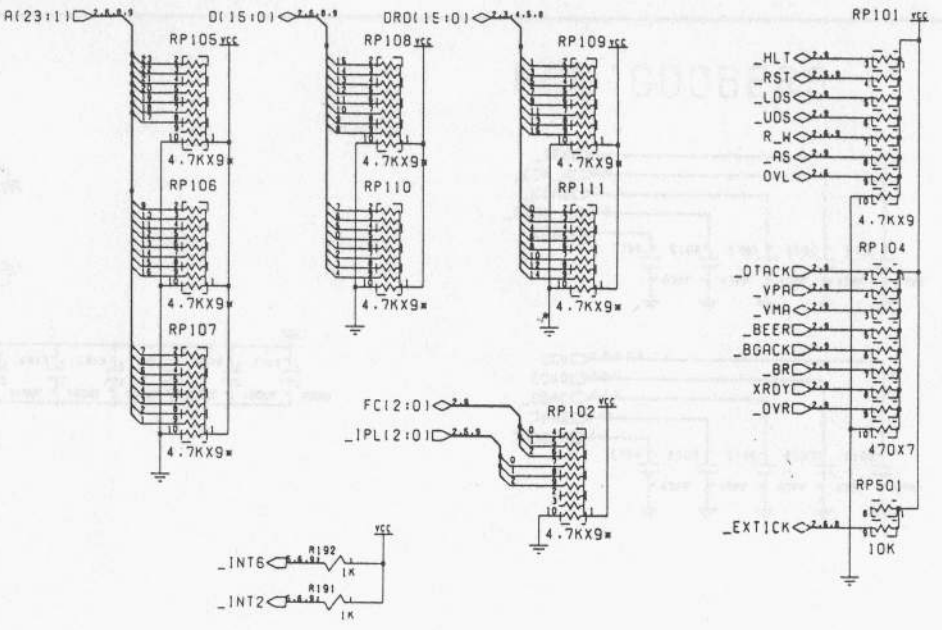
SHEET 3 OF 10


VIDEO POWER
NOTE: PIN 2 AND 21 OF HY1 CONNECTED INTERNALLY
U4
DENISE HR
8373
U40
U41
74HCT245
HY1
VIDEO
HYBRID
HY1A
COLOR
ANNEX
VIDEO
CN9
D823S
CN10
COMPOSITE
JP11
DRD(15:0)
RGA(8:1)
MOV
MOH
M1V
M1H
CCK
_CSYNC
_CDAC
7MHZ_A
C403
47PF
_VSYNC
_HSYNC
_XCLKEN
XCLK
CCK_C
PIXLSW
NOTE: R409 CONTROLS COMPOSITE OUTPUT
LEVEL FOR 390229-01 HYBRID.
AUDIO POWER
A500 REV 8 PCB
NOTE: COMPONENTS DESIGNATED AS EXXX MAY BE LOADED
WITH EMI FLITERS, FERRITE BEADS OR RESISTORS!
DENISE IS PRETTY MUCH INTO VIDEO...
COMMODORE
SCHEMATIC A500 REV 8
A500 MAIN BOARD
"ROCK LOBSTER"
312813 0

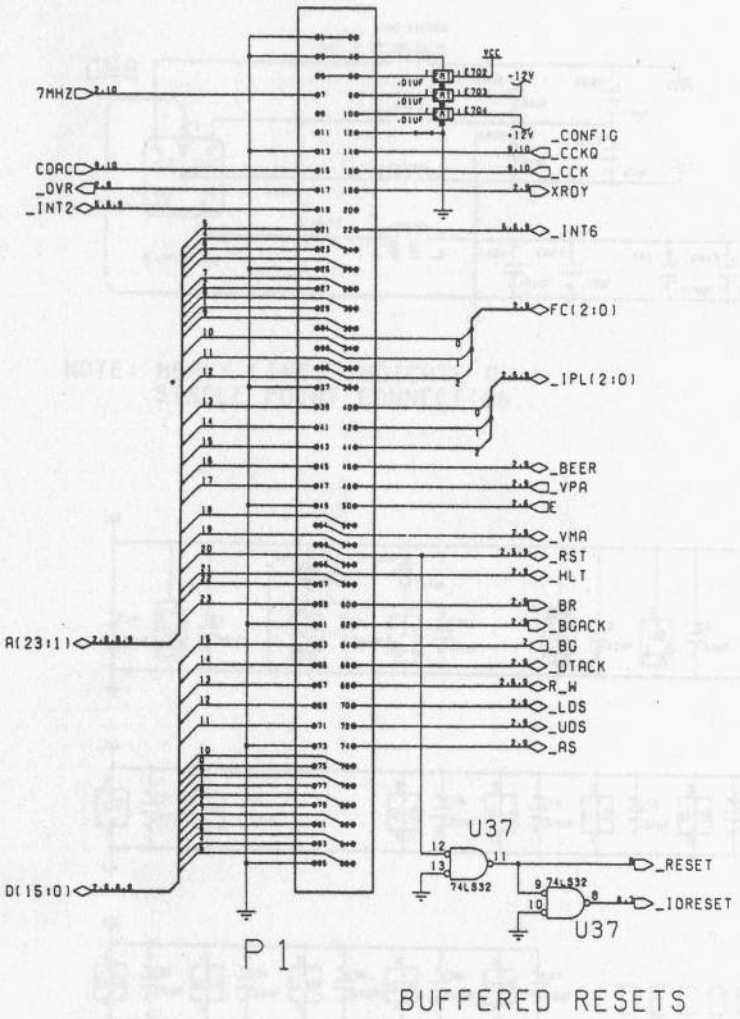

LEFT JOY
CN1
RIGHT JOY
CN2
D89P
JP8
_FIRE0
_LPEN
_FIRE1
POT0Y
POT0X
POT1Y
POT1X
4.7 1/2W
R401
R408
4.7KX9
RP401
74LS157
U15
_CCKQ_A
MOV
MOH
M1V
M1H
MOUSE/JOYSTICK PORTS
U3
8364
PAULA
_IPL(2:0)
DRD(15:0)
RGA(8:1)
DMAL
CCK
CCKQ
_RST
_INT6
_INT3
_INT2
_RXD
_TXD
_DKRD
_DKWD
_DKWE
R305
FB802
NOTE: GROUND INTERCONNECTION NEAR AUDIO JACKS.
AUDIO FILTERS
JP10A
AUDIN
R339
C331
R331
U14
LF347
/TL084
VREF
RIGHT
E305
270PF
C332
R332
R333
Q331
MPF102
R336
C333
C335
C334
R334
R335
E303
CN3
JP10B
AUDOUT
LEFT
E306
C321
R321
C322
R322
R323
Q321
R326
C323
C325
C324
R324
R325
E302
CN4
_LED
1488
U38
R307
R308
2N3906
Q301
C308
NOTE: LED OFF, FILTERS BYPASSED
TODO: ANALYZE ANALOG
PAULA PREFERS THE TRADITIONAL MODES
COMMODORE
SCHEMATIC A500 REV 8
C/A500 MAIN BOARD
"ROCK LOBSTER"
C 312813 0
A500 REV 8 PCB


RS232 DECOUPLING
U39
C39
.01UF
U38
+12V
-12V
RP501
10K
U7
8520
VIA
D[15:0]
A[23:1]
_KBDATA
_KBCLOCK
_FIRE1
_FIRE0
_RDY
_TRK0
_WPROT
_CHNG
_LED
_OVL
_ODD_CIA
_INT2
_VSYNC
_EXTICK
JP7B
PP0[7:0]
CN7
DB25S
_IORESET
PARALLEL PORT
Q501
2N3904
R502
2.7K
R501
10K
1N914
D501
U8
8520
VIA
U38
U39
1489
1488
_TXD
_RXD
RS232
DB25P
CN6
.33UF
C501
AUDIN
C502
AUDOUT
_EVEN_CIA
R_W
E
R109
68
_INT6
_HSYNC
_RESET
_MTR
_SEL3
_SEL2
_SEL1
_SEL0
_SIDE
DIR
_STEP
RP501
10K
_INDEX
A500 REV 8 PCB
NOTE: E501-503 ARE LOADED WITH 47 OHM 1/2 W RESISTORS
RS232, PARALLEL PORT AND KEYBOARD
COMMODORE
SCHEMATIC A500 REV 8
A500 MAIN BOARD
ROCK LOBSTER
312813

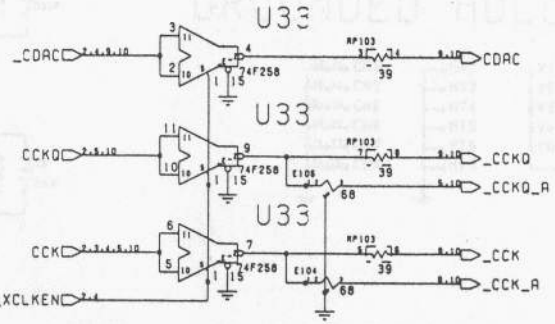
# EXPANSION BUS TERMINATION AND PULLUPS




# EXPANSION BUS




# CLOCK DISTRIBUTION




# BUFFERED RESETS

A500 REV 8 PCB

NOTE: RP105-RP111 ARE OPTIONAL INTERNAL BUS TERMINATION, AND ARE NOT NORMALLY LOADED.

EXPANSION BUS AND CLOCK DISTIBUTION

COMMODORE

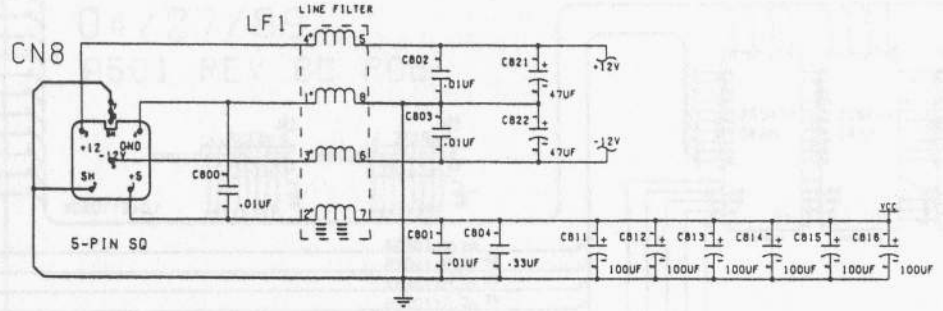
SCHEMATIC A500 REV 8
"A500 MAIN BOARD
"ROCK LOBSTER"

312813 8

SCALE

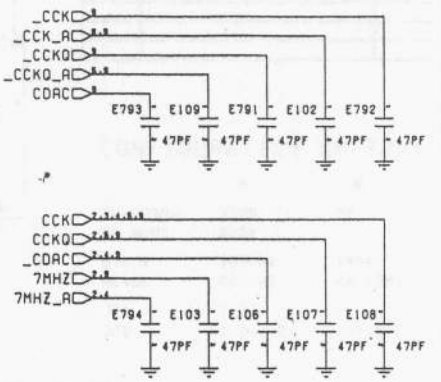
SHT 9 OF 10

# POWER INPUT

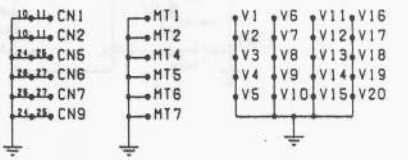


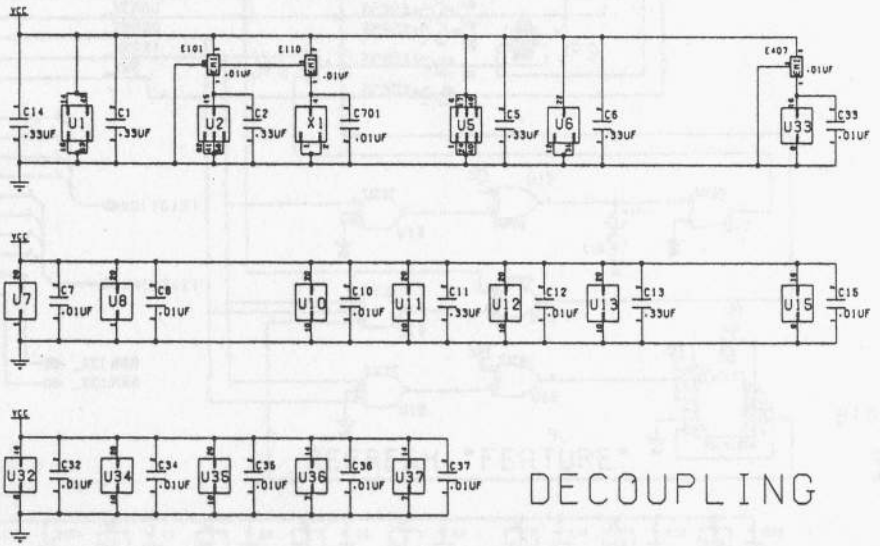

NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION

# FCC GOOBERS




# GROUNDED HOLES, &C.




# DECOUPLING

# SPARES

RP103 39

RP103 39

# A500 REV 8 PCB

POWER DISTRIBUTION AND DECOUPLING

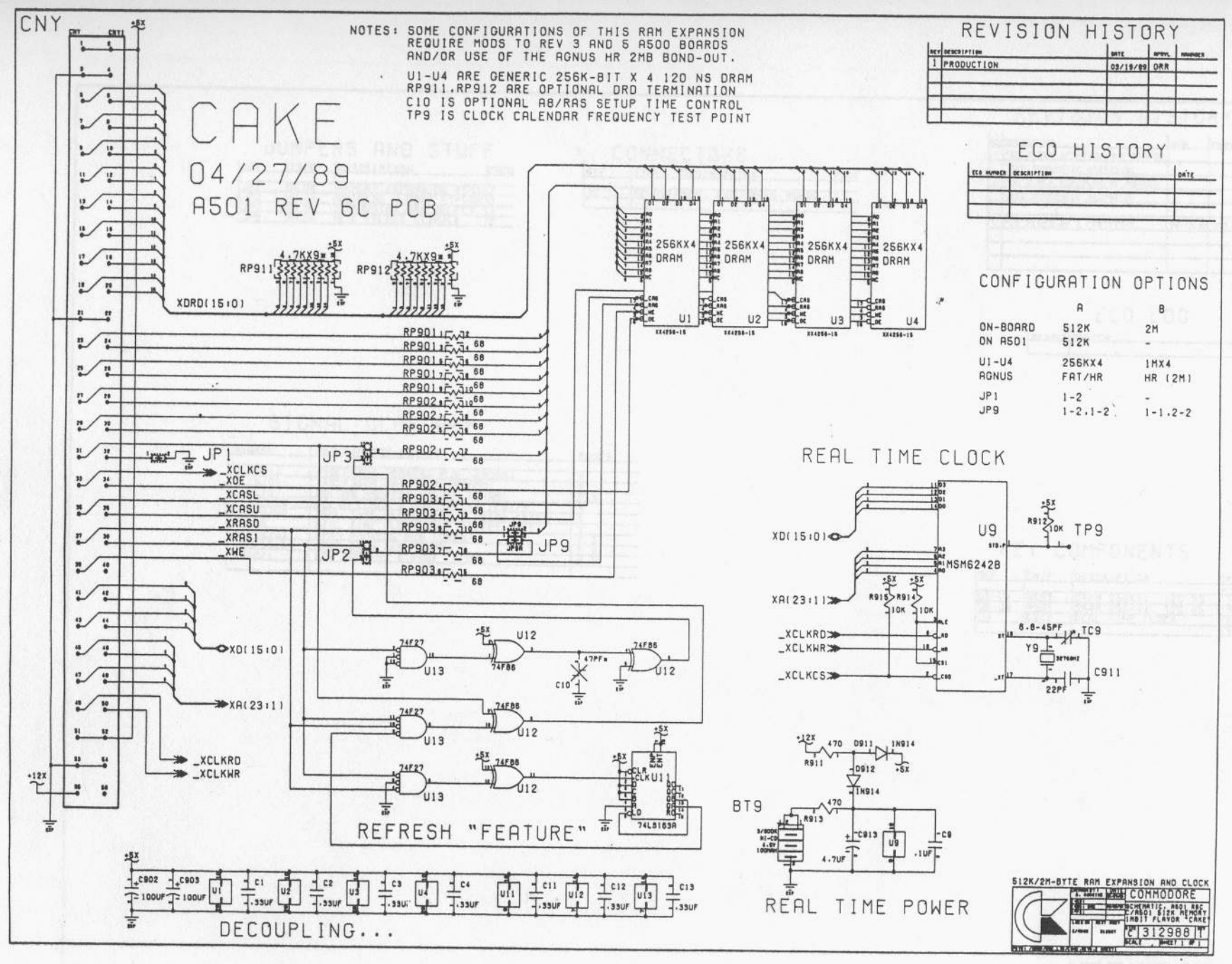
COMMODORE

SCHEMATIC A500 REV 8
C/A500 MAIN BOARD
"ROCK LOBSTER"

C 312813 0

SCALE

SHEET 10 OF 10


CNY
NOTES: SOME CONFIGURATIONS OF THIS RAM EXPANSION REQUIRE MODS TO REV 3 AND 5 A500 BOARDS AND/OR USE OF THE AGNUS HR 2MB BOND-OUT.
U1-U4 ARE GENERIC 256K-BIT X 4 120 NS DRAM
RP911,RP912 ARE OPTIONAL DRD TERMINATION
C10 IS OPTIONAL A8/RAS SETUP TIME CONTROL
TP9 IS CLOCK CALENDAR FREQUENCY TEST POINT
REVISION HISTORY
REV DESCRIPTION DATE APPVL NUMBER
1 PRODUCTION 03/19/89 ORR
ECO HISTORY
ECO NUMBER DESCRIPTION DATE
CAKE
04/27/89
A501 REV 6C PCB
RP911 4.7KX9
RP912 4.7KX9
XDRD(15:0)
256KX4 DRAM
U1
U2
U3
U4
CONFIGURATION OPTIONS
A B
ON-BOARD 512K 2M
ON A501 512K -
U1-U4 256KX4 1MX4
AGNUS FAT/HR HR (2M)
JP1 1-2 -
JP9 1-2,1-2 1-1,2-2
JP1
JP2
JP3
JP9
_XCLKCS
_XOE
_XCASL
_XCASU
_XRAS0
_XRAS1
_XWE
XD(15:0)
XA(23:1)
_XCLKRD
_XCLKWR
+12X
REAL TIME CLOCK
U9
MSM62428
TP9
R912 10K
R915 10K
R914 10K
6.8-45PF
TC9
Y9
C911
22PF
REFRESH "FEATURE"
74F27
74F86
74LS163A
C10 47PF
BT9
R911 470
D911 1N914
D912 1N914
R913 470
C913 4.7UF
C9 .1UF
REAL TIME POWER
DECOUPLING...
C902 100UF
C903 100UF
C1 .33UF
C2 .33UF
C3 .33UF
C4 .33UF
C11 .33UF
C12 .33UF
C13 .33UF
512K/2M-BYTE RAM EXPANSION AND CLOCK
COMMODORE
SCHEMATIC, A501 REV C/A501 512K MEMORY EXPANSION WITH CLOCK, 1MBIT FLAVOR "CAKE"
C 312988 1
SCALE
SHEET 1 OF 1

## JUMPERS AND STUFF

| REF | TYPE | DESCRIPTION | PAGE |
|---|---|---|---|
| JP1 | BLOB | MEMORY EXPANSION SENSE | 3 |
| JP2 | BLOB | REFRESH KLUDGE BYPASS | 2 |
| JP3 | BLOB | EXPANSION RAS SELECT | 2 |
| JP9 | BLOB | RTC SELECT DISABLE | 3 |

## CONNECTORS

| REF | TYPE | DESCRIPTION | PAGE |
|---|---|---|---|
| J9 | 56-RAFH | MEM. EXP. MAIN-BOARD | 3 |

## REVISION HISTORY

| REV | DESCRIPTION | DATE | APRVL | MANAGER |
|---|---|---|---|---|
| - | FOR OLDER REVISION 3/5 BOARDS | | | |
| | SEE SCHEMATIC 312511-01 | | | |
| - | FOR OLDER REVISION 6C BOARDS | | | |
| | SEE SCHEMATIC 312988-01 | | | |
| | | | | |
| 0 | PCB REVISION 8 PROTOTYPE | 05/13/91 | ORR | |
| | | | | |
| | | | | |
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## ECO LOG

| ECO NUMBER | DESCRIPTION | DATE |
|---|---|---|
| | | |

## SIGNAL GLOSSARY

| SIGNAL | DESCRIPTION (AREA) | PAGES |
|---|---|---|
| A[23:1] | PROCESSOR ADDRESS BUS (68000) | 3 |
| D[15:0] | PROCESSOR DATA BUS (68000) | 3 |
| CASL/U | COLUMN ADDRESS STROBE (DRAM) | 2,3 |
| CCK/CCKQ | COLOR CLOCK / QUADRATURE (CHIPS) | 3 |
| CLKRD/WR | REAL TIME CLOCK READ / WRITE (RTC) | 3 |
| CLKCS | REAL TIME CLOCK CHIP SELECT (RTC) | 3 |
| DRA[8:0] | DRAM ADDRESS BUS (DRAM) | 2,3 |
| DRD[15:0] | DRAM DATA BUS (DRAM) | 2,3 |
| RASO/1 | ROW ADDRESS STROBE (DRAM) | 2,3 |

## KEY COMPONENTS

| REF | CHIP | DESCRIPTION | PAGE |
|---|---|---|---|
| U1-U4 | ASST | DRAM 256KX4, 120 NS | 3 |
| U5-U8 | ASST | DRAM 256KX4, 120 NS | 3 |
| U9 | 6242 | REAL TIME CLOCK | 6 |
| | | | 5 |

A PAGE FOR PERVEEN AND LARRY TO USE

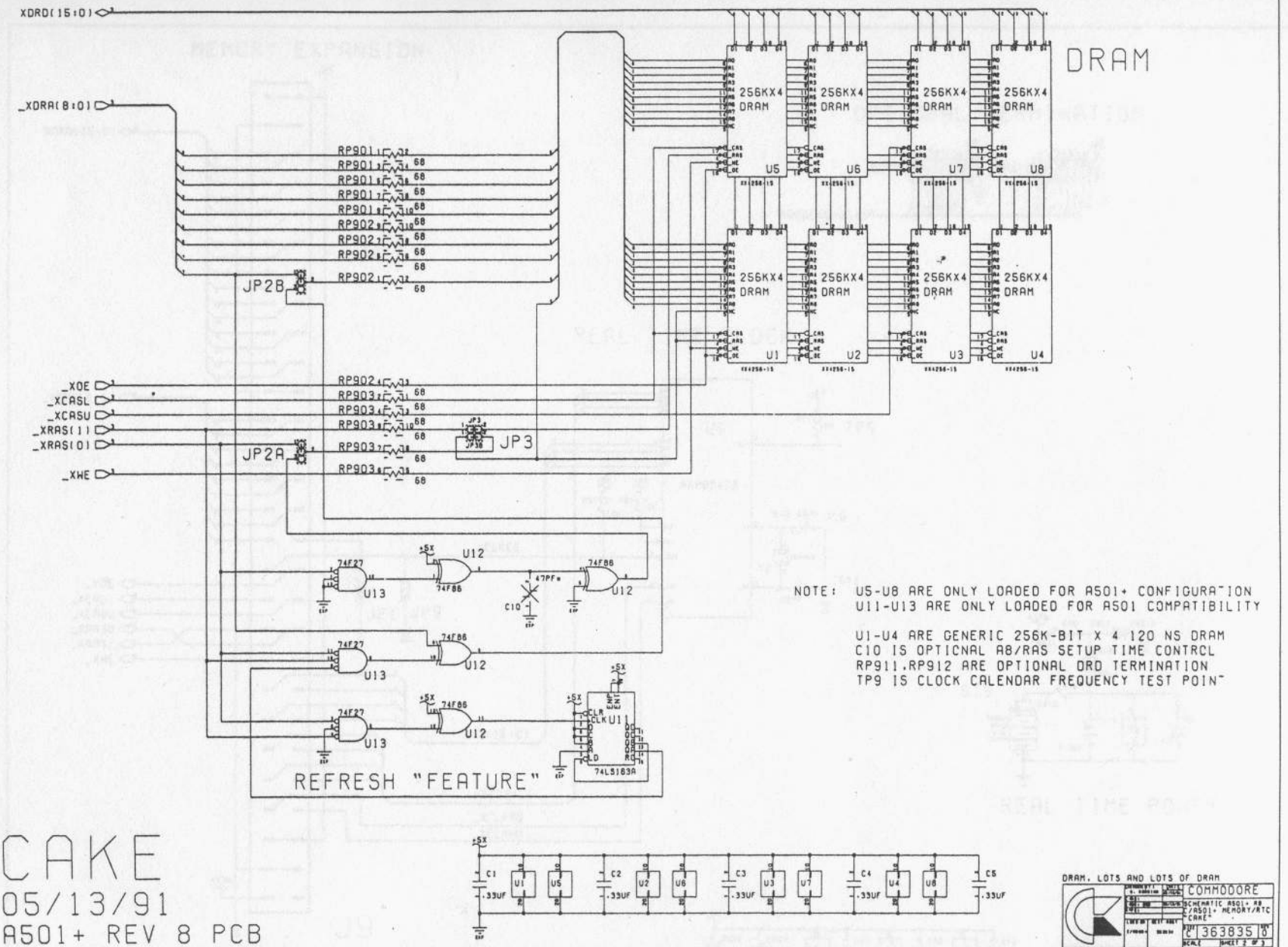
COMMODORE

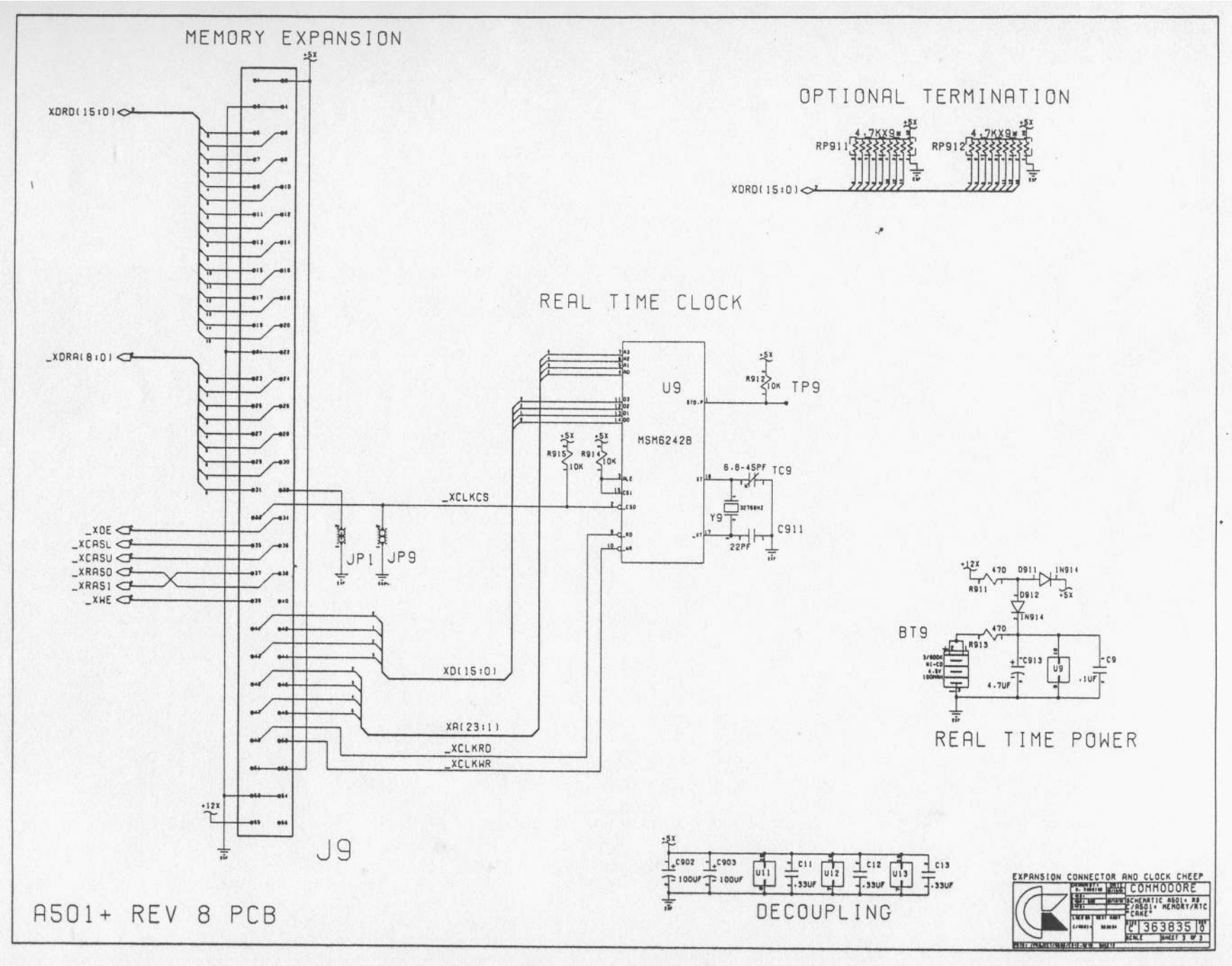
SCHEMATIC A501+ A8 C/A501+ MEMORY/RTC + CAGE

P.C. 363835 0

SCALE SHEET 1 OF 3

# A501+ REV 8 PCB


XDRD(15:0)
_XDRA(8:0)
DRAM
256KX4 DRAM
U1
U2
U3
U4
U5
U6
U7
U8
RP901
RP902
RP903
68
JP2B
JP2A
JP3
_XOE
_XCASL
_XCASU
_XRAS(1)
_XRAS(0)
_XWE
74F27
74F86
74LS163A
U11
U12
U13
C10
47PF
REFRESH "FEATURE"
NOTE: U5-U8 ARE ONLY LOADED FOR A501+ CONFIGURATION
U11-U13 ARE ONLY LOADED FOR A501 COMPATIBILITY
U1-U4 ARE GENERIC 256K-BIT X 4 120 NS DRAM
C10 IS OPTICNAL A8/RAS SETUP TIME CONTRCL
RP911,RP912 ARE OPTIONAL DRD TERMINATION
TP9 IS CLOCK CALENDAR FREQUENCY TEST POIN
CAKE
05/13/91
A501+ REV 8 PCB
C1
C2
C3
C4
C5
.33UF
DRAM, LOTS AND LOTS OF DRAM
COMMODORE
363835


MEMORY EXPANSION
XDRD(15:0)
_XDRA(8:0)
_XOE
_XCASL
_XCASU
_XRAS0
_XRAS1
_XWE
_XCLKCS
JP1
JP9
XD(15:0)
XA(23:1)
_XCLKRD
_XCLKWR
+12V
+5V
J9
OPTIONAL TERMINATION
RP911
RP912
4.7KX9
REAL TIME CLOCK
U9
MSM6242B
R912
10K
TP9
R915
R914
6.8-45PF
TC9
Y9
32768HZ
22PF
C911
REAL TIME POWER
BT9
R911
470
D911
IN914
D912
R913
C913
4.7UF
.1UF
DECOUPLING
C902
C903
100UF
C11
C12
C13
.33UF
A501+ REV 8 PCB
EXPANSION CONNECTOR AND CLOCK CHEEP
COMMODORE
SCHEMATIC A501+ REV 8
C/A501+ MEMORY/RTC
CARE
363835
SHEET 3 OF 3