

SIGNAL	DESCRIPTION
28MHZ	28.63636 MHz (NTSC)/28.37516 MHz (PAL) Master Clock
7MHZ	7 MHz Processor Clock
A[23:1]	Processor Address (68000)
ACK	Data Acknowledge (Parallel)
AS	Address Strobe (68000)
AUDIN	Audio Input (RS232 jack)
AUDOUT	Audio Output (RS232 jack)
BEER	Bus Error (68000)
BG	Bus Grant (68000)
BGACK	Bus Grant Acknowledge (68000)
BLISS	Blitter Slowdown (chips)
BLIT	Chip Memory Access (chips)
BR	Bus Request (68000)
BUSY	Device Busy (parallel)
CASL/CASU	CAS lower/upper byte (DRAM)
CCK	Color Clock aka C1 (chips)
CCKQ	Color Clock Quadrature aka C3 (chips)
CDAC	7 MHz Quadrature Clock
CHNG	Media Change (floppy)
CLKRD/CLKWR	Real-time Clock Read/Write
CSYNC	Composite Sync (video)
CTS	Clear to Send (rs232)
D[15:0]	Processor Data (68000)
DIR	Direction (floppy)
DKRD	Diskette Read Data (floppy)
DKWDB	Diskette Write Data (floppy)
DKWEB	Diskette Write Enable (floppy)
DMAL	Chip DMA Request (chips)
DRA[8:0]	DRAM Address (DRAM, chips)
DRD[15:0]	DRAM Data (DRAM, chips)
DSR	Data Set Ready (rs232)
DTACK	Data Transfer Acknowledge (68000)
DTR	Data Terminal Ready (rs232)
E	Peripheral E Clock (68000)
EXRAM	Expansion Memory Present
FC[0:0]	Function Control (68000)
FIRE0/FIRE1	Fire Button (joysticks)
HLT	Processor Halt (68000)
HSYNC	Horizontal Sync (video)
INDEX	Diskette Index Hole (floppy)
INT[2,3,6]	Interrupt Requests (chips)
I/O RESET	I/O Reset
IPL[2:0]	Processor Interrupt Requests (68000)
KBCLOCK	Keyboard Clock (keyboard)
KBDATA	Keyboard Data (keyboard)
KBRESET	Keyboard Reset (keyboard)
LDS/UDS	Upper/Lower Data Strobe (68000)
LED	Power On LED

SIGNAL	DESCRIPTION
LEFT/RIGHT	Audio Channels
MTR	Motor On (floppy)
MTR0	Motor On Drive (floppy)
MOV/MOH	Mouse Quadrature Signals (joysticks)
MIV/MIH	Mouse Quadrature Signals (joysticks)
OVL	Overlay ROM over RAM
OVR	Override System Decoding
PIXELSW	Pixel Switch (video)
POT0X/POT0Y	Pot Lines (joysticks)
POT1X/POT1Y	Pot Lines (joysticks)
POUT	Paper Out (parallel)
PPD[7:0]	Parallel Port Data (parallel)
RAMEN	RAM Enable (chips)
REGEN	Chip Register Enable (chips)
RAS0/RAS1	RAS Internal/Expansion Lines (DRAM)
RDY	Drive Ready (floppy)
RESET	General Reset
RGA[8:1]	Register Address Bus (chips)
RI	Ring Indicate (rs232)
ROMEN	ROM Enable
RTS	Request to Send (rs232)
RST	Processor Reset (68000)
RXD	Receive Data (RS232)
RW	Processor Read/Write (68000)
SEL	Select (parallel)
SEL[3:0]	Drive Select (floppy)
SIDE	Side Select (floppy)
STEP	Head Step Command (floppy)
TRK0	Track 0 Sense (floppy)
TXD	Transmit Data (RS232)
VMA	Valid Memory Address (68000)
VPA	Valid Peripheral Address (68000)
VSYNC	Vertical Sync (video)
WE	Write Enable (DRAM)
WPROT	Write Protect Sense (floppy)
XCLK	External 28 MHz Clock (genlock)
XCLKEN	External Clock Enable (genlock)
XRDY	External Data Ready
AUDL/AUDR	Amiga Audio Left/Right
AEMP	Audio Deemphasis
AUPLY	CD Audio Play
BAS	Buffered Address Strobe
BCLK	CD Audio Clock
BCSMCEN/BCSMCOD	Buffered Chip Select Memory Card Even/Odd
BRW	Buffered Processor Read/Write
BSEN	Logic Voltage Sense
BTXD	Buffer Transmit Data (Mid)
BLDS/BUDS	Buffered Upper/Lower Data Strobe

SIGNAL	DESCRIPTION
C16M	16MHz Dac Clock
CDAL/CDAR	CD Audio Left/Right
CD/TV	Select CD/TV (see INCD)
CONFIGIN	Config In
CONFIGOUT	Config Out
CSCD	Chip Select CDROM Driver
CSEN/CSOD	Chip Select CDROM Driver Even/Odd
CSMC	Chip Select Memory Card
CSMCEN/CSMCOD	Chip Select Memory Card Even/Odd
CSNV	Non-Volatile Memory Select
CSRC	Real Time Chip Select
CSX0	XT Device Chip Select No.0
DACATT	Attinator Data (Dac)
DACLCH	Attinator Latch (Dac)
DACST	Attinator Strobe (Dac)
DATA	CD Audio Data
DMCD	Dmac Dma Data
EOP_CSX1	End of Process/XT Device Chip Select No.1
GMS[1:0]	Genlock Mode Select (Remote Control)
IFRST	Interface Reset
INAC	Indicator Power/Status
INCD	Indicator CD/TV Mode
INTD	CD Drive Reset
INTS	SCSI Interrupt
IOR/IOW	Dmac Read/Write
KBSE	Keyboard Sense
LMUTE	Line Mute
LRCLK	Audio Left/Right Clock
MPS	Power Sense (Logic)
MS[1:0]	Genlock Mode Select (Amiga)
MUTE	CD Mute
POWER	Main Logic Power On/Off
SD[7:0]	Dmac XT/SCSI Data
VCK	Attinator Data Clock (Head Phone)
VDATA	Attinator Data Clock (Head Phone)
VF[2:1]	Filament Voltage
VST	Attinator Data Clock (Head Phone)
VFP	-30V Voltage
XA, YA, XB, YB[2:1]	Mouse Input Signal
XDACK	XT Device Data Acknowledge
XDREQ	XT Device Data Requirement
EMC	ENABLE MEMORY CARD
ECD	ENABLE CDROM DRIVER (ROM)
WEPROM	WRITE ENABLE E ² FROM





















