SNES S-PPU2 Pinout by Jonathon W. Donaldson (jwdonal) (special thanks to Martin Korth (nocash))

Designator	Name	Desc	QFP100P1870X2470-64AM	Type	Owner	Show	Number	Name
1	B\U\R\S\T\	Video Output Color Burst Strobe (Active-Low) (to-S-ENC)	1	Output	1	True	True	B\U\R\S\T\
2	P\E\D\	Unknown (NC)	2	Passive	1	True	True	P\E\D\
3	3.58M	Video Output Clock (3.58MHz) (NTSC) (to S-ENC)	3	Output	1	True	True	3.58M
4	T\O\U\M\E\I\	Unknown (NC)	4	Passive	1	True	True	T\O\U\M\E\I\
5	VCC	Supply	5	Power	1	True	True	VCC
6	P\A\W\R\	5A22 B-Bus Write Strobe (Active-Low)	6	Input	1	True	True	P\A\W\R\
7	P\A\R\D\	5A22 B-Bus Read Strobe (Active-Low)	7	Input	1	True	True	P\A\R\D\
8	D7	5A22 Data Bus	8	I/O	1	True	True	D7
9	D6	5A22 Data Bus	9	I/O	1	True	True	D6
10	D5	5A22 Data Bus	10	I/O	1	True	True	D5
11	D4	5A22 Data Bus	11	I/O	1	True	True	D4
12	D3	5A22 Data Bus	12	I/O	1	True	True	D3
13	D2	5A22 Data Bus	13	I/O	1	True	True	D2
14	D1	5A22 Data Bus	14	I/O	1	True	True	D1
15	D0	5A22 Data Bus	15	I/O	1	True	True	D0
16	GND	Supply	16	Power	1	True	True	GND
17	PA7	5A22 B-Bus Address	17	Input	1	True	True	PA7
18	PA6	5A22 B-Bus Address	18	Input	1	True	True	PA6
19	PA5	5A22 B-Bus Address	19	Input	1	True	True	PA5
20	PA4	5A22 B-Bus Address	20	Input	1	True	True	PA4
21	PA3	5A22 B-Bus Address	21	Input	1	True	True	PA3
22	PA2	5A22 B-Bus Address	22	Input	1	True	True	PA2
23	PA1	5A22 B-Bus Address	23	Input	1	True	True	PA1
24	PA0	5A22 B-Bus Address	24	Input	1	True	True	PA0
25	HBLANK	Horizontal Blank (to 5A22)	25	Output	1	True	True	HBLANK
26	VBLANK	Vertical Blank (to 5A22)	26	Output	1	True	True	VBLANK
27	5\M\O\U\T\	Dot Clock Out (5.37MHz) (to expansion port)	27	Passive	1	True	True	5\M\O\U\T\
28	R\E\S\O\U\T\1\	Reset Out 1 (to CPU, APU, Cartridge, Expansion port, etc.)	28	Output	1	True	True	R\E\S\O\U\T\1\
29	EXTLATCH	External Latch (Lightpen signal) (to Joypad)	29	I/O	1	True	True	EXTLATCH
30	PALMODE	PAL Video Mode Enable (VCC=PAL, GND=NTSC) (GND)	30	Input	1	True	True	PALMODE
31	XIN	Master Clock (21.47727MHz) (from Osc)	31	Input	1	True	True	XIN
32	VCC	Supply	32	Power	1	True	True	VCC
33	R\E\S\O\U\T\0\	Reset Out 0 (to PPU1)	33	Output	1	True	True	R\E\S\O\U\T\0\
34	R\E\S\E\T\	Reset In (from CIC)	34	Input	1	True	True	R\E\S\E\T\
35	GND	Supply	35	Power	1	True	True	GND
36	FIELD	Unknown (connected to PPU1)	36	Passive	1	True	True	FIELD
37	O\V\E\R\1\	Unknown (connected to PPU1)	37	Input	1	True	True	O\V\E\R\1\

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38	5\M\I\N\	Dot Clock In (5.37MHz) (from PPU1)	38	Passive	1	True	True	5\M\I\N\	
39	H\C\L\D\	Unknown (connected to PPU1)	39	Passive	1	True	True	H\C\L\D\	
40	V\C\L\D\	Unknown (connected to PPU1)	40	Passive	1	True	True	V\C\L\D\	
41	COLOR0	Unknown (connected to PPU2)	41	Passive	1	True	True	COLOR0	
42	COLOR1	Unknown (connected to PPU2)	42	Passive	1	True	True	COLOR1	
43	COLOR2	Unknown (connected to PPU2)	43	Passive	1	True	True	COLOR2	
44	PRIO0	Unknown (connected to PPU2)	44	Passive	1	True	True	PRIO0	
45	PRIO1	Unknown (connected to PPU2)	45	Passive	1	True	True	PRIO1	
46	CHR0	Unknown (connected to PPU2)	46	Passive	1	True	True	CHR0	
47	CHR1	Unknown (connected to PPU2)	47	Passive	1	True	True	CHR1	
48	CHR2	Unknown (connected to PPU2)	48	Passive	1	True	True	CHR2	
49	CHR3	Unknown (connected to PPU2)	49	Passive	1	True	True	CHR3	
50	O\V\E\R\2\	Unknown (connected to local /OVER1, and /OVER on PPU1)	50	Input	1	True	True	O\V\E\R\2\	
51	VDB0	VRAM Data Bus (High Byte)	51	I/O	1	True	True	VDB0	
52	VDB1	VRAM Data Bus (High Byte)	52	I/O	1	True	True	VDB1	
53	VDB2	VRAM Data Bus (High Byte)	53	I/O	1	True	True	VDB2	
54	VDB3	VRAM Data Bus (High Byte)	54	I/O	1	True	True	VDB3	
55	VDB4	VRAM Data Bus (High Byte)	55	I/O	1	True	True	VDB4	
56	VDB5	VRAM Data Bus (High Byte)	56	I/O	1	True	True	VDB5	
57	VDB6	VRAM Data Bus (High Byte)	57	I/O	1	True	True	VDB6	
58	VDB7	VRAM Data Bus (High Byte)	58	I/O	1	True	True	VDB7	
59	VCC	Supply	59	Power	1	True	True	VCC	
60	VDA0	VRAM Data Bus (Low Byte)	60	I/O	1	True	True	VDA0	
61	VDA1	VRAM Data Bus (Low Byte)	61	I/O	1	True	True	VDA1	
62	VDA2	VRAM Data Bus (Low Byte)	62	I/O	1	True	True	VDA2	
63	VDA3	VRAM Data Bus (Low Byte)	63	I/O	1	True	True	VDA3	
64	VDA4	VRAM Data Bus (Low Byte)	64	I/O	1	True	True	VDA4	
65	VDA5	VRAM Data Bus (Low Byte)	65	I/O	1	True	True	VDA5	
66	VDA6	VRAM Data Bus (Low Byte)	66	I/O	1	True	True	VDA6	

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67	VDA7	VRAM Data Bus (Low Byte)	67	I/O	1	True	True	VDA7
68	GND	Supply	68	Power	1	True	True	GND
69	EXT0	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	69	Input	1	True	True	EXT0
70	EXT1	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	70	Input	1	True	True	EXT1
71	EXT2	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	71	Input	1	True	True	EXT2
72	EXT3	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	72	Input	1	True	True	EXT3
73	EXT4	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	73	Input	1	True	True	EXT4
74	EXT5	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	74	Input	1	True	True	EXT5
75	EXT6	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	75	Input	1	True	True	EXT6
76	EXT7	External Video Input (from VRAM Data Bus (High Byte)) (it is unclear why this is wired up to VRAM in SNES)	76	Input	1	True	True	EXT7
77	TST0	Unknown (NC)	77	Passive	1	True	True	TST0
78	TST1	Unknown (NC)	78	Passive	1	True	True	TST1
79	TST2	Unknown (NC)	79	Passive	1	True	True	TST2
80	TST3	Unknown (NC)	80	Passive	1	True	True	TST3
81	TST4	Unknown (NC)	81	Passive	1	True	True	TST4
82	TST5	Unknown (NC)	82	Passive	1	True	True	TST5
83	VCC	Supply	83	Power	1	True	True	VCC
84	TST6	Unknown (NC)	84	Passive	1	True	True	TST6
85	TST7	Unknown (NC)	85	Passive	1	True	True	TST7
86	TST8	Unknown (NC)	86	Passive	1	True	True	TST8
87	TST9	Unknown (NC)	87	Passive	1	True	True	TST9
88	TST10	Unknown (NC)	88	Passive	1	True	True	TST10
89	TST11	Unknown (NC)	89	Passive	1	True	True	TST11
90	TST12	Unknown (NC)	90	Input	1	True	True	TST12
91	TST13	Unknown (NC)	91	Input	1	True	True	TST13

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92	TST14	Unknown (NC)	92	Input	1	True	True	TST14	
93	TST15	Unknown (NC)	93	Input	1	True	True	TST15	
94	AVCC	Supply	94	Passive	1	True	True	AVCC	
95	R	Analog Red Component (to S-ENC)	95	Output	1	True	True	R	
96	G	Analog Green Component (to S-ENC)	96	Output	1	True	True	G	
97	B	Analog Blue Component (to S-ENC)	97	Output	1	True	True	B	
98	HVCMODE	Home Video Computer (a.k.a. Famicom) Mode (purpose unknown since SNES can play Famicom games already) (GND)	98	Input	1	True	True	HVCMODE	
99	GND	Supply	99	Power	1	True	True	GND	
100	C\S\Y\N\C\	Video Output Composite Sync (Active-Low) (to S-ENC)	100	Output	1	True	True	C\S\Y\N\C\	