SNES S-CPU Pinout by Jonathon W. Donaldson (jwdonal) (special thanks to Martin Korth (nocash))

Designator	Name	Desc	QFP100P1870X2470-64AM	Type	Owner	Show	Number	Name
1	VCC	Supply	1	Power	1	True	True	VCC
2	CA8	A-Bus Address	2	Output	1	True	True	CA8
3	CA9	A-Bus Address	3	Output	1	True	True	CA9
4	CA10	A-Bus Address	4	Output	1	True	True	CA10
5	CA11	A-Bus Address	5	Output	1	True	True	CA11
6	CA12	A-Bus Address	6	Output	1	True	True	CA12
7	CA13	A-Bus Address	7	Output	1	True	True	CA13
8	CA14	A-Bus Address	8	Output	1	True	True	CA14
9	CA15	A-Bus Address	9	Output	1	True	True	CA15
10	CA16	A-Bus Address	10	Output	1	True	True	CA16
11	CA17	A-Bus Address	11	Output	1	True	True	CA17
12	CA18	A-Bus Address	12	Output	1	True	True	CA18
13	CA19	A-Bus Address	13	Output	1	True	True	CA19
14	CA20	A-Bus Address	14	Output	1	True	True	CA20
15	CA21	A-Bus Address	15	Output	1	True	True	CA21
16	CA22	A-Bus Address	16	Output	1	True	True	CA22
17	CA23	A-Bus Address	17	Output	1	True	True	CA23
18	GND	Supply	18	Power	1	True	True	GND
19	JPIO0	NC	19	I/O	1	True	True	JPIO0
20	JPIO1	NC	20	I/O	1	True	True	JPIO1
21	JPIO2	NC	21	I/O	1	True	True	JPIO2
22	JPIO3	NC	22	I/O	1	True	True	JPIO3
23	JPIO4	NC	23	I/O	1	True	True	JPIO4
24	JPIO5	NC	24	I/O	1	True	True	JPIO5
25	JPIO6	Port 4201h/4213h	25	I/O	1	True	True	JPIO6
26	JPIO7	Port 4201h/4213h	26	I/O	1	True	True	JPIO7
27	4017.D0	4017h.Read.Bit0	27	Input	1	True	True	4017.D0
28	4017.D1	4017h.Read.Bit1	28	Input	1	True	True	4017.D1
29	4017.D2	4017h.Read.Bit2 (GND)	29	Input	1	True	True	4017.D2
30	4017.D3	4017h.Read.Bit3 (GND)	30	Input	1	True	True	4017.D3
31	4017.D4	4017h.Read.Bit4 (GND)	31	Input	1	True	True	4017.D4
32	4016.D0	4016h.Read.Bit0	32	Input	1	True	True	4016.D0
33	4016.D1	4016h.Read.Bit1	33	Input	1	True	True	4016.D1
34	VCC	Supply	34	Power	1	True	True	VCC
35	JPCLK1	4016h.Read (Joypad Clock)	35	Output	1	True	True	JPCLK1
36	JPCLK2	4017h.Read (Joypad Clock)	36	Output	1	True	True	JPCLK2
37	JPOUT0	4016h.Write.Bit0 (Joypad Strobe))	37	Output	1	True	True	JPOUT0
38	JPOUT1	NC	38	Output	1	True	True	JPOUT1
39	JPOUT2	NC	39	Output	1	True	True	JPOUT2
40	REFRESH	DRAM Refresh for WRAM, four HIGH pulses per scanline	40	Output	1	True	True	REFRESH
41	TCKSEL0	Unknown (GND)	41	Input	1	True	True	TCKSEL0
42	TCKSEL1	Unknown (GND)	42	Input	1	True	True	TCKSEL1
43	HBLANK	For H/V-timers and V-Blank NMI (from PPU2)	43	Input	1	True	True	HBLANK
44	VBLANK	For H/V-timers and V-Blank NMI (from PPU2)	44	Input	1	True	True	VBLANK
45	N\M\I\	VCC	45	Input	1	True	True	N\M\I\
46	I\R\Q\	Interrupt Request (Active-Low) (from Cartridge and Expansion	46	Input	1	True	True	I\R\Q\

Designator	Name	Desc	QFP100P1870X2470-64AM	Type	Owner	Show	Number	Name
		Port)						
47	GND	Supply	47	Power	1	True	True	GND
48	XIN	Master Clock (21.47727MHz) (from Osc)	48	Input	1	True	True	XIN
49	D\R\A\M\M\O\D\E\	GND (used to disable DRAM refresh)	49	Input	1	True	True	D\R\A\M\M\O\D\E\
50	R\E\S\E\T\	Reset (from System)	50	Input	1	True	True	R\E\S\E\T\
51	PA0	B-Bus Address	51	Output	1	True	True	PA0
52	PA1	B-Bus Address	52	Output	1	True	True	PA1
53	PA2	B-Bus Address	53	Output	1	True	True	PA2
54	PA3	B-Bus Address	54	Output	1	True	True	PA3
55	PA4	B-Bus Address	55	Output	1	True	True	PA4
56	PA5	B-Bus Address	56	Output	1	True	True	PA5
57	PA6	B-Bus Address	57	Output	1	True	True	PA6
58	PA7	B-Bus Address	58	Output	1	True	True	PA7
59	VCC	Supply	59	Power	1	True	True	VCC
60	D0	Data Bus	60	I/O	1	True	True	D0
61	D1	Data Bus	61	I/O	1	True	True	D1
62	D2	Data Bus	62	I/O	1	True	True	D2
63	D3	Data Bus	63	I/O	1	True	True	D3
64	D4	Data Bus	64	I/O	1	True	True	D4
65	D5	Data Bus	65	I/O	1	True	True	D5
66	D6	Data Bus	66	I/O	1	True	True	D6
67	D7	Data Bus	67	I/O	1	True	True	D7
68	P\A\R\D\	B-Bus Read Strobe (Active-Low)	68	Output	1	True	True	P\A\R\D\
69	P\A\W\R\	B-Bus Write Strobe (Active-Low)	69	Output	1	True	True	P\A\W\R\
70	D\M\A\	NC	70	Output	1	True	True	D\M\A\
71	CPUCK	NC	71	Output	1	True	True	CPUCK
72	SYSCK	System Clock (most likely the current memory access cycle clock, i.e. 3.58MHz, 2.68MHz, or 1.79MHz) (to WRAM and Cartridge)	72	Output	1	True	True	SYSCK
73	TM	Unknown (GND)	73	Input	1	True	True	TM
74	HVCMODE	Home Video Computer (a.k.a. Famicom) Mode (purpose unknown since SNES can play Famicom games already) (GND)	74	Input	1	True	True	HVCMODE
75	HALT	Unknown (GND)	75	Input	1	True	True	HALT
76	A\B\O\R\T\	VCC	76	Input	1	True	True	A\B\O\R\T\
77	R\O\M\S\E\L\	ROM Select (Access to 00-3F/80-BF:8000-FFFF or 40-7D/C0-FF:0000-FFFF) (to Cartridge)	77	Output	1	True	True	R\O\M\S\E\L\
78	R\A\M\S\E\L\	WRAM Select (Access to 00-3F/80-BF:0000-1FFF or 7E-7F:0000-FFFF)	78	Output	1	True	True	R\A\M\S\E\L\
79	GND	Supply	79	Power	1	True	True	GND
80	R/W\	NC	80	Output	1	True	True	R/W\
81	RDY	VCC	81	Input	1	True	True	RDY
82	M\L\	Memory Lock (Active-Low) (asserted on read/modify/write	82	Output	1	True	True	M\L\

Designator	Name	Desc	QFP100P1870X2470-64AM		Type	Owner	Show	Number	Name
		instructions to inform other ics that the bus may not be claimed yet) (NC)							
83	MF	CPU Status Register M-Flag (NC)	83	Output	1	True	True	MF	
84	XF	CPU Status Register X-Flag (NC)	84	Output	1	True	True	XF	
85	VCC	Supply	85	Power	1	True	True	VCC	
86	VPA	Valid Program Address (along with VDA, encodes 1 of 4 possible processor states) (NC)	86	Output	1	True	True	VPA	
87	VDA	Valid Program Address (along with VDA, encodes 1 of 4 possible processor states) (NC)	87	Output	1	True	True	VDA	
88	ALCK	Unknown (appears to be the inverse of pin71 or pin72) (NC)	88	Output	1	True	True	ALCK	
89	V\P\	Vector Pull (Active-Low) (asserted whenever exception vector addresses ($00:FFE4-FFEF, $00:FFF4-FFFF) are being accessed)	89	Output	1	True	True	V\P\	
90	GND	Supply	90	Power	1	True	True	GND	
91	C\P\U\W\R\	A-Bus Write Strobe (Active-Low)	91	Output	1	True	True	C\P\U\W\R\	
92	C\P\U\R\D\	A-Bus Read Strobe (Active-Low)	92	Output	1	True	True	C\P\U\R\D\	
93	CA0	A-Bus Address	93	Output	1	True	True	CA0	
94	CA1	A-Bus Address	94	Output	1	True	True	CA1	
95	CA2	A-Bus Address	95	Output	1	True	True	CA2	
96	CA3	A-Bus Address	96	Output	1	True	True	CA3	
97	CA4	A-Bus Address	97	Output	1	True	True	CA4	
98	CA5	A-Bus Address	98	Output	1	True	True	CA5	
99	CA6	A-Bus Address	99	Output	1	True	True	CA6	
100	CA7	A-Bus Address	100	Output	1	True	True	CA7	