SNES S-SMP Pinout by Jonathon W. Donaldson (jwdonal) (special thanks to Martin Korth (nocash))

Designator	Name	Desc	QFP100P1870X2470-64AM	Type	Owner	Show	Number	Name
1	CPUA4	SRAM Address (to S-DSP)	1	Output	1	True	True	CPUA4
2	CPUA3	SRAM Address (to S-DSP)	2	Output	1	True	True	CPUA3
3	CPUA2	SRAM Address (to S-DSP)	3	Output	1	True	True	CPUA2
4	CPUA1	SRAM Address (to S-DSP)	4	Output	1	True	True	CPUA1
5	CPUA0	SRAM Address (to S-DSP)	5	Output	1	True	True	CPUA0
6	CPUD7	SRAM Data (to/from S-DSP)	6	I/O	1	True	True	CPUD7
7	CPUD6	SRAM Data (to/from S-DSP)	7	I/O	1	True	True	CPUD6
8	CPUD5	SRAM Data (to/from S-DSP)	8	I/O	1	True	True	CPUD5
9	CPUD4	SRAM Data (to/from S-DSP)	9	I/O	1	True	True	CPUD4
10	CPUD3	SRAM Data (to/from S-DSP)	10	I/O	1	True	True	CPUD3
11	CPUD2	SRAM Data (to/from S-DSP)	11	I/O	1	True	True	CPUD2
12	CPUD1	SRAM Data (to/from S-DSP)	12	I/O	1	True	True	CPUD1
13	CPUD0	SRAM Data (to/from S-DSP)	13	I/O	1	True	True	CPUD0
14	PD3	CPUK Clock-Enable used to create effective SMP frequency of 1.024MHz (from S-DSP)	14	Input	1	True	True	PD3
15	PD2	MD Bus tri-state control signal used when S-SMP is accessing SRAM (to S-DSP)	15	Output	1	True	True	PD2
16	CPUK	2.048MHz (from S-DSP)	16	Input	1	True	True	CPUK
17	P\5\R\D\	Unknown (likely just unneeded signal from commercial Sony SPC700) (NC)	17	Output	1	True	True	P\5\R\D\
18	P57	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	18	I/O	1	True	True	P57
19	P56	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	19	I/O	1	True	True	P56
20	P55	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	20	I/O	1	True	True	P55
21	P54	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	21	I/O	1	True	True	P54
22	P53	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	22	I/O	1	True	True	P53
23	P52	Unknown (likely just	23	I/O	1	True	True	P52

Designator	Name	Desc	QFP100P1870X2470-64AM	Type	Owner	Show	Number	Name
		unneeded port from commercial Sony SPC700) (NC)						
24	P51	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	24	I/O	1	True	True	P51
25	P50	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	25	I/O	1	True	True	P50
26	VSS	Supply	26	Power	1	True	True	VSS
27	P47	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	27	I/O	1	True	True	P47
28	P46	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	28	I/O	1	True	True	P46
29	P45	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	29	I/O	1	True	True	P45
30	P44	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	30	I/O	1	True	True	P44
31	P43	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	31	I/O	1	True	True	P43
32	P42	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	32	I/O	1	True	True	P42
33	P41	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	33	I/O	1	True	True	P41
34	P40	Unknown (likely just unneeded port from commercial Sony SPC700) (NC)	34	I/O	1	True	True	P40
35	T1	Unknown (maybe test or timer?) (tied to VCC)	35	Input	1	True	True	T1
36	T0	Unknown (maybe test or timer?) (tied to VCC)	36	Input	1	True	True	T0
37	R\E\S\E\T\	Reset (Active-Low) (from System)	37	Input	1	True	True	R\E\S\E\T\
38	D7	I/O Port Data (to/from 5A22 B-Bus Data)	38	I/O	1	True	True	D7
39	D6	I/O Port Data (to/from 5A22 B-Bus Data)	39	I/O	1	True	True	D6
40	D5	I/O Port Data (to/from 5A22 B-Bus Data)	40	I/O	1	True	True	D5
41	D4	I/O Port Data (to/from 5A22 B-Bus Data)	41	I/O	1	True	True	D4

Designator	Name	Desc	QFP100P1870X2470-64AM		Type	Owner	Show	Number	Name
42	D3	I/O Port Data (to/from 5A22 B-Bus Data)	42	I/O	1	True	True	D3	
43	D2	I/O Port Data (to/from 5A22 B-Bus Data)	43	I/O	1	True	True	D2	
44	D1	I/O Port Data (to/from 5A22 B-Bus Data)	44	I/O	1	True	True	D1	
45	D0	I/O Port Data (to/from 5A22 B-Bus Data)	45	I/O	1	True	True	D0	
46	R\D\	I/O Port Read (Active-Low) (from 5A22 B-Bus /PARD))	46	Input	1	True	True	R\D\	
47	W\R\	I/O Port Write (Active-Low) (from 5A22 B-Bus /PAWR)	47	Input	1	True	True	W\R\	
48	A1	I/O Port Address (from 5A22 B-Bus Address PA1)	48	Input	1	True	True	A1	
49	A0	I/O Port Address (from 5A22 B-Bus Address PA0)	49	Input	1	True	True	A0	
50	CS	I/O Port Chip-Select (from 5A22 B-Bus PA6)	50	Input	1	True	True	CS	
51	C\S\	I/O Port Chip-Select (Active-Low) (from 5A22 B-Bus PA7)	51	Input	1	True	True	C\S\	
52	CPUA15	SRAM Address (to S-DSP)	52	Output	1	True	True	CPUA15	
53	CPUA14	SRAM Address (to S-DSP)	53	Output	1	True	True	CPUA14	
54	CPUA13	SRAM Address (to S-DSP)	54	Output	1	True	True	CPUA13	
55	CPUA12	SRAM Address (to S-DSP)	55	Output	1	True	True	CPUA12	
56	CPUA11	SRAM Address (to S-DSP)	56	Output	1	True	True	CPUA11	
57	VCC	Supply	57	Power	1	True	True	VCC	
58	VSS	Supply	58	Power	1	True	True	VSS	
59	CPUA10	SRAM Address (to S-DSP)	59	Output	1	True	True	CPUA10	
60	CPUA9	SRAM Address (to S-DSP)	60	Output	1	True	True	CPUA9	
61	CPUA8	SRAM Address (to S-DSP)	61	Output	1	True	True	CPUA8	
62	CPUA7	SRAM Address (to S-DSP)	62	Output	1	True	True	CPUA7	
63	CPUA6	SRAM Address (to S-DSP)	63	Output	1	True	True	CPUA6	
64	CPUA5	SRAM Address (to S-DSP)	64	Output	1	True	True	CPUA5	